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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,885	06/26/2001	Mark T. Ramsbey	F0279	2423

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EXAMINER	
MAGEE, THOMAS J	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/891,885	Applicant(s) RAMSBEY ET AL.	
	Examiner Thomas J. Magee	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-13 and 15-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-13 and 15-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Cancellations

1. Applicant's cancellation of Claim 14 in Letter No. 13 of March 20, 2003 is acknowledged. Claims 9 – 13, and 15 - 18 are pending and still active.

Claim Rejections – 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 9,10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fliesler et al. (US 6,238,975 B1) in view of Huang (US 5,378,649), and Sakakibara (US 6,445,617 B1).

Fliesler et al. disclose a non-volatile memory device (Col. 7, lines 6 – 34) having a core and a peripheral region on a substrate where one or more insulating regions for one or more ESD transistors are provided in the peripheral region with a polysilicon (gate) layer formed over the insulating layers. After patterning the ESD and other transistors spacers are formed surrounding the gate structures. (Col. 2, lines 41 – 43, Col. 5, lines 9 – 14, Col. 7, lines 28 – 32, Figure 4). Heavy doping is then done in ESD transistors while also doping other transistors in the peripheral region (Col. 2, lines 1 – 12), where

the deployment of spacers prior to subsequent or heavy implants is obvious and consistent with routine procedure in the art (Sakakibara, Figures 3A to 3D, Col. 11, lines 45 – 54).

Fliesler et al. do not disclose the use of polysilicon word lines in the core region, wherein the word lines are separated by about 1um or less. Huang discloses that the polycrystalline word lines used in a nonvolatile memory device are spaced at a distance in the range, 0.2 to 0.5um, consistent with the value recited in the instant application. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Huang with Fliesler et al. to obtain polysilicon word lines at appropriate spacings to reduce crosstalk and coupling.

4. Claims 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fliesler et al., as applied to Claims 9,10, and 15 above, and further in view of Diaz et al. ("Building –in ESD/EOS Reliability for Sub-half Micron CMOS Processes," Proc. 33rd Reliability Physics Symp., 4 – 6 April, 1995, pp.276 – 283).

Fliesler et al. disclose (Col. 2, lines 27 – 29) a heavy implant of phosphorus to a dose of of 3 x 10(^)15/cm(^)2 , but do not disclose the ion energy. In a similar application with a similar structure, Diaz et al. disclose (Table 2, page 279) that the ion energy is 65 keV. In both cases, the parameters are well within the range of values recited in the instant application. Further, it would have been obvious at the time of the invention to one of ordinary skill in the art to combine Diaz et al. with Fliesler et al. to obtain an optimum ion implant condition to deploy in the memory circuit.

5. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fliesler et al., as applied to Claims 9, 10, and 15 above, and further in view of Reisinger (6,008,081).

Fliesler et al. do not explicitly disclose that the flash memory array is a SONOS type structure, but this would have been an easy modification. SONOS cells have been present since the late 1960's, although newer dielectric layers have been utilized in recent applications. Reisinger discloses (Col. 8, lines 5 – 12) the formation of MOS transistors with multiplayer dielectrics (51,52,53) capped by a polysilicon layer (6) (See Figure 1) to produce a classical SONOS structure. Hence, it would have been obvious at the time of the invention to one of ordinary skill in the art to add Reisinger to Fliesler et al. to obtain a SONOS gate dielectric structure with improved dielectric properties in the flash memory circuit.

6. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fliesler et al. in view of Diaz et al, Huang, and Sakakibara.

As discussed earlier, Fliesler et al. disclose the formation of a non-volatile semiconductor memory device (Col. 7, lines 6 – 34) where a core and peripheral region are established with ESD and other transistors containing one or more insulating layers formed in the peripheral region. A polysilicon layer is formed over the insulating layers and subsequent patterning done prior to formation of spacer material and etching to define edge spacers. The source and drain regions are lightly doped (Col. 1, lines 66 –

67) with phosphorus (Col. 7, lines 60 – 61). The deployment of spacers prior to subsequent or heavy implants is obvious and consistent with routine procedure in the art (Sakakibara, Figures 3A to 3D, Col. 11, lines 45 – 54).

Fliesler et al . do not explicitly disclose the implant energy/dose product, but Diaz et al. in a similar ESD transistor construction (Table 2, page 279) disclose for both standard (control) and LDD phosphorus implants, an implant energy in the range, 25 to 50 keV, with total doses in the range, 5 x 10(^)13/cm(^)2 to 10(^)14/cm(^)2, well within the energy-dose product recited in the instant application. With the spacers in place and masks provided over core and peripheral regions, heavy ion implants are done through an opening over the peripheral region (Col. 7, lines 17 – 25) into sources and drains (Col.2, lines 41 – 43, Col. 5, lines 9 – 14, Col. 7, lines 28 – 32, Figure 4).

Again, Fliesler et al. do not explicitly disclose the energy-dose product for the heavy implant, but do disclose a maximum dose in the range, 3 x 10(^)15 to 6 x 10(^)15/ cm(^)2 (Col. 7, lines 54 – 56). Diaz et al. disclose (Table 2) both the energy (50 to 65 keV) and the dose (4 x 10(^)14 to 10(^)15/cm(^)2) used in the heavy implants, both of which are well within the range recited in the instant application.

It would have been obvious at the time of the invention to one of ordinary skill in the art to combine the implant parameters of Diaz et al. with the ESD transistors of Fliesler et al. to produce working devices in the non-volatile memory circuit.

Fliesler et al. do not disclose the use of polysilicon word lines in the core region, wherein the word lines are separated by about 1um or less. Huang discloses that the polycrystalline word lines used in a nonvolatile memory device are spaced at a distance in the

range, 0.2 to 0.5um, consistent with the value recited in the instant application. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Huang with Fliesler et al. to obtain polysilicon word lines at appropriate spacings to reduce crosstalk and coupling.

Response to Arguments

7. Applicant's arguments with respect to claims 9 – 13, and 15 – 18 have been considered but have been found to be unpersuasive and moot in view of the new ground(s) of rejection. Some comments should be made, however, in regard to arguments presented by Applicant. Applicant has apparently either misread or misunderstood the use of spacers in the Fliesler et al. reference. One of the embodiments incorporates spacers on the sides of the gate structure prior to heavy ion implantation (Col. 5, lines 9 – 14) (See also Claims 3 and 4) Figure 4 clearly shows that the spacer is acting as a boundary for the heavy implant, where the spacer is formed prior to the heavy implant. This is routine in the art (See Sakakibara, (Figure 3A to 3D)).

For informational purposes, metal word lines have been used in non-volatile memories for almost three decades (See Arnett et al., US 4,068,217) such that polysilicon/silicides are not the only material used. The Wilson reference is valid for a number of conducting materials and simply points out the dependence of crosstalk coupling on spacing.

Conclusions

8. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305 5396.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Tom Thomas**, can be reached on **(703) 308-2772.**. The fax number for the organization where this application or proceeding is assigned is **(703) 308-7722.**

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
April 1, 2003